PCI-DAS1000, PCI-DAS1001 & PCI-DAS1002

Multifunction Analog & Digital I/O

User's Manual

MEASUREMENT COMPUTING™

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1 Introduction

The PCI-DAS1000, PCI-DAS1001 and PCI-DAS1002 are multifunction analog and digital I/O boards designed to operate in computers with PCI bus accessory slots. The boards have the following capabilities:

- 16 single-ended or eight differential analog inputs with sample rates as high as 250 kHz.
- 24-bits of parallel digital I/O
- Three, user-accessible, 16-bit counters.
- Two analog output channels (PCI-DAS1001 and PCI-DAS1002 only)

The board's analog input ranges are as follows:

PCI-DAS1000, PCI-DAS1002	Bipolar:	±10V, ±5V, ±2.5V, and ±1.25V
	Unipolar:	0 to 10V, 0 to 5V, 0 to 2.5V and 0 to 1.25V
PCI-DAS1001	Bipolar:	±10V, ±1.0V, ±0.1V, ±0.01V
	Unipolar:	0 to 10V, 0 to 1.0V, 0 to 0.1V, 0 to 0.01V

The PCI-DAS1000 series is fully plug-and-play with no switches or jumpers to set. The boards are self-calibrating with no potentiometers to adjust. All calibration is performed via software and on-board trim D/A converters.

The PCI-DAS1000 series is fully supported by the powerful Universal Library software as well as a wide variety of application software packages including SoftWIRE.

NOTE:

Unless a specific model code is required, this manual references the PCI-DAS1000 as a general term.

2 Installation

2.1 Software Installation

The board has no switches or jumpers to set. The simplest way to configure your board is to use the InstaCal™ program provided on the CD (or floppy disk). InstaCal™ will create a configuration file that your application software (and the optional Universal Library™) will refer to so the software you use will automatically have access to the exact configuration of the board.

Please refer to the *Software Installation Manual* regarding the installation and operation of InstaCal.

2.2 Hardware Installation

The PCI-DAS1000 series boards are completely plug and play. There are no switches or jumpers to set. Configuration is controlled by your systems' BIOS. Follow the steps shown below to install your PCI board.

WARNING

Do not unplug the computer when installing the board. Doing so removes the computer's ground.

1. Turn your computer off, open it up, and insert the PCI-DAS1000 board into any available PCI slot.
2. Close your computer up and turn it on.
3. If you are using an operating system with support for Plug and Play (such as Windows 95 or 98), a dialog box will pop up as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for a disk containing it. The InstaCal software supplied with your board contains this file. Insert the disk or CD and click OK.

2.3 Connector Pinout Diagrams

The PCI-DAS1000 series boards use a 100-pin I/O connector. See Figures 2-1 and 2-2 for the PCI-DAS1000.
See Figures 2-3 and 2-4 for the PCI-DAS1001 and PCI-DAS1002, 8-channel differential and 16-channel single ended respectively.

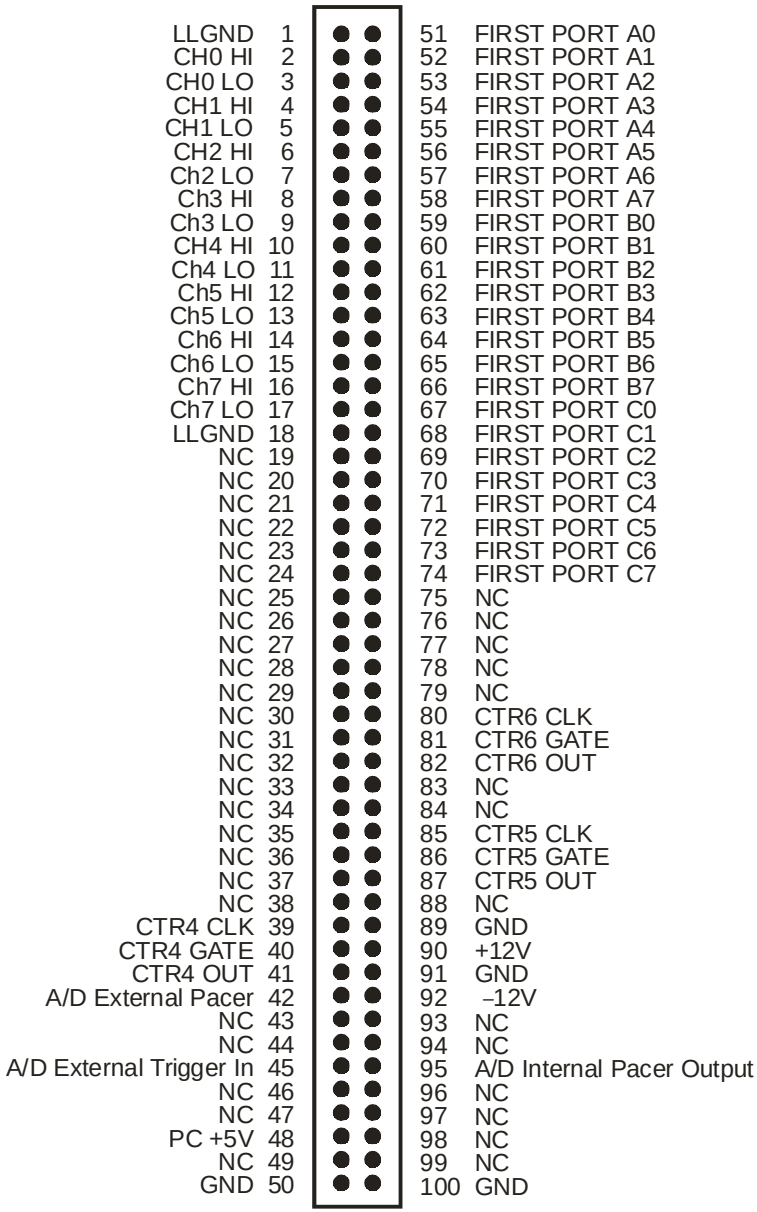


Figure 2-1. Connector Diagram for PCI-DAS1000 - 8-Channel Differential Usage

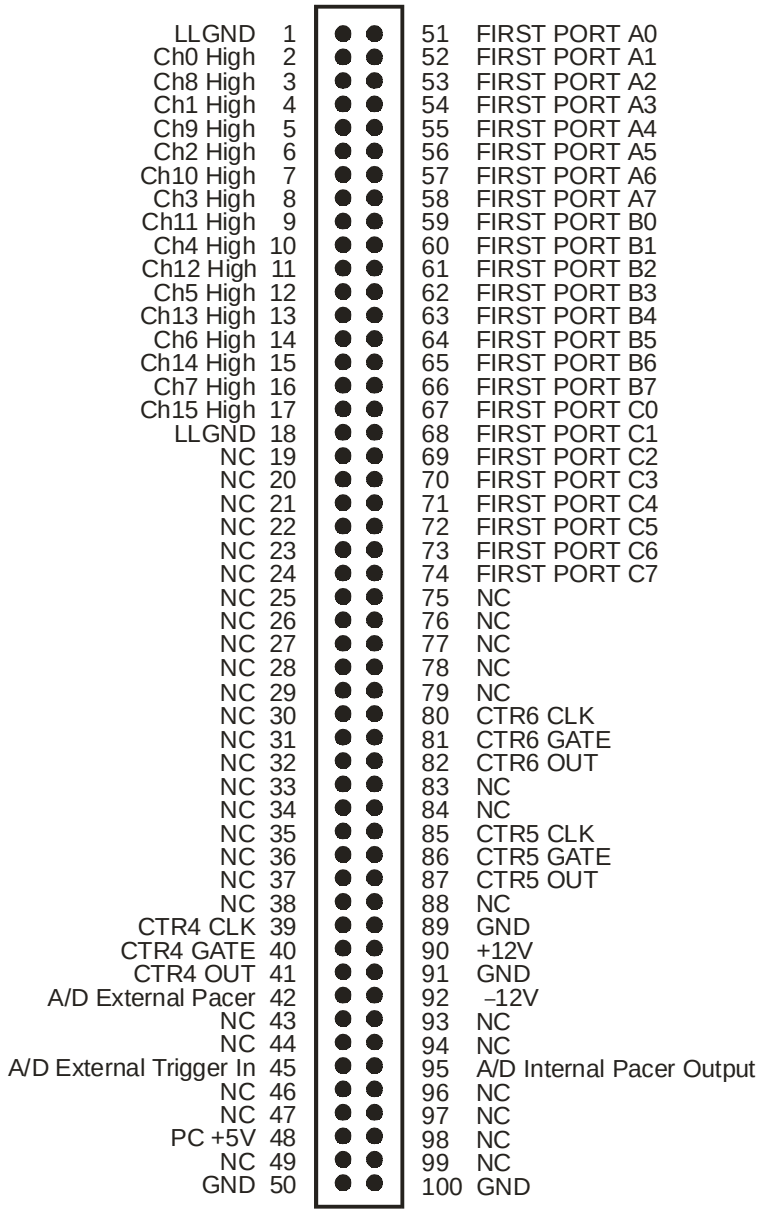


Figure 2-2. Connector Diagram for PCI-DAS1000 - 16-Channel Single-Ended Usage

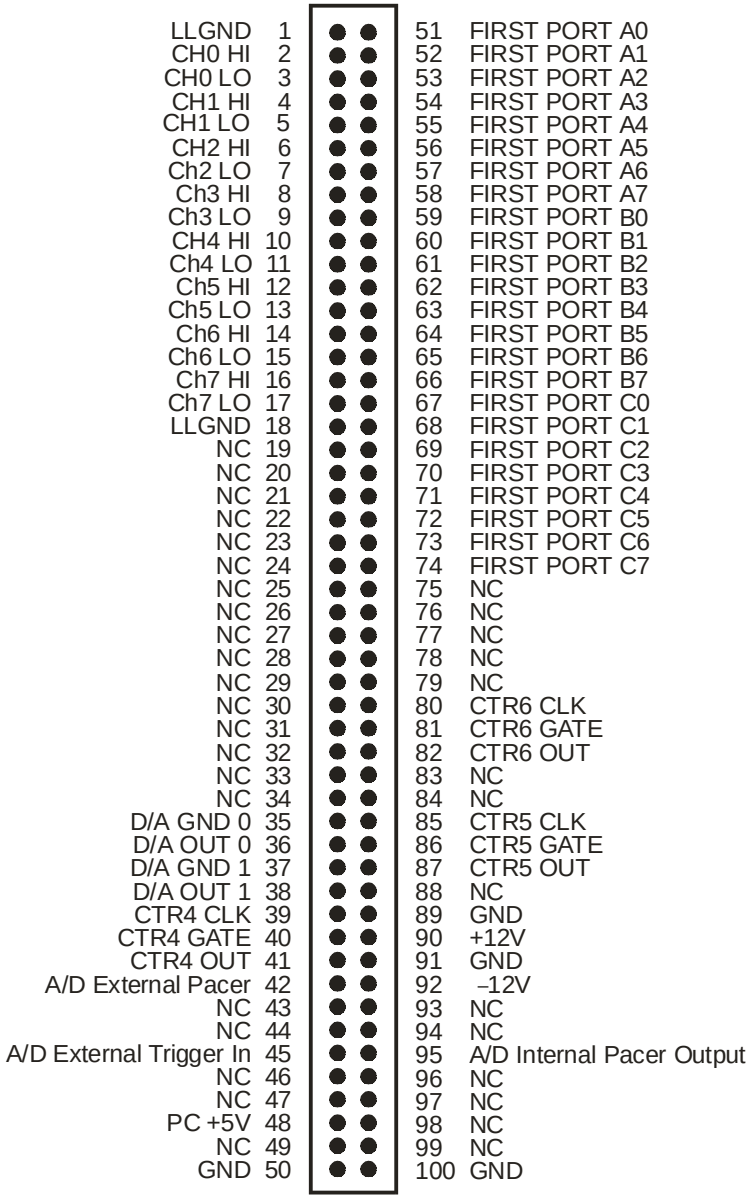
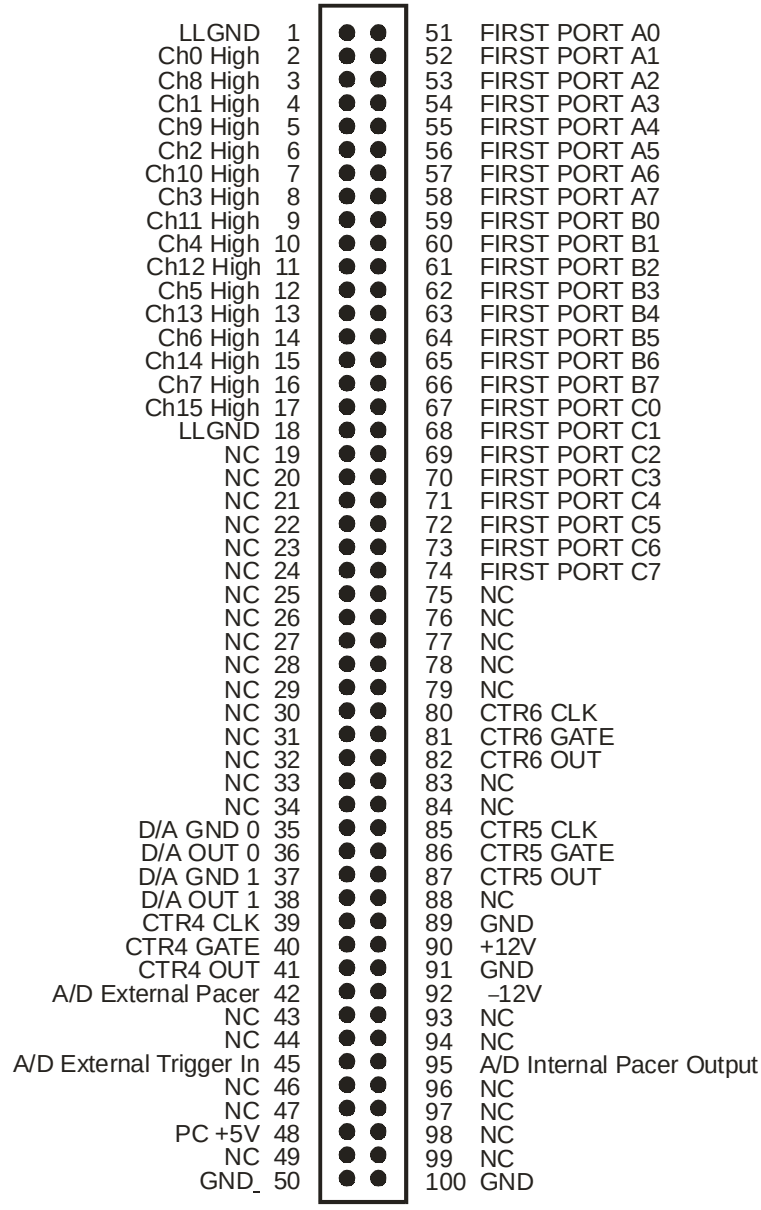


Figure 2-3. Connector Diagram for PCI-DAS1001 & 1002 - 8-Channel Differential Usage



PCI-DAS1001 & PCI-DAS1002 Connector Diagram
16 Channel, Single-Ended

Figure 2-4. Connector Diagram for PCI-DAS1001 & 1002 - 16-Channel Single-EndedUsage

2.4 Connecting Signals to the PCI-DAS1000

The 100-pin connector provides a far greater signal density than the traditional 37-pin D-type connector. For a mating cable, use the C100FF-2. This cable assembly has a 100-pin connector that fans out to a pair of 50-pin ribbon cables. The two 50-pin ribbon cable legs are terminated with standard 50-pin header connectors. A pair of CIO-MINI50 screw terminal boards, a single CIO-TERM100 screw terminal board or a single SCB-50 breakout box can be used to terminate field signals and route them to the PCI-DAS1000. The BNC16/8 series interface box provides convenient and reliable BNC connections to each of the analog outputs.

There is additional information regarding analog signal connection and configuration at http://www.measurementcomputing.com/signals/signals.pdf.

3 Programming & Applications

3.1 Programming Languages

The Universal Library provides complete access to the PCI-DAS1000 functions from the full range of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic or any other language, please refer to the Universal Library manual.

3.2 Packaged Application Programs

Many packaged application programs, such as SoftWIRE have drivers for the PCI-DAS1000. If the software you use does not have drivers for the PCI-DAS1000, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain the necessary drivers.

Some application drivers are included with the Universal Library package, but not with the Application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us for more information on this topic.

3.3 Register Level Programming

The PCI-DAS1000 is supported by the powerful Universal Library. We strongly recommend that you take advantage of the Universal Library as your software interface. The complexity of registers used for automatic calibration, combined with the PCI BIOS's dynamic allocation of addresses and internal resources, make the PCI-DAS1000 series challenging to program via direct register I/O operations. Direct I/O programming should be attempted only by experienced programmers.

Although the PCI-DAS1000 is part of the larger DAS family, there is no correspondence between register locations of the PCI-DAS1000 and boards in the CIO-DAS16 family. Software written at the register level for the other DAS boards will not work with the PCI-DAS1000. However, software based on the Universal Library should work with the PCI-DAS1000 with few or no changes.

If you decide that register level programming is required for your application, information on the register functions can be found at
http://www.measurementcomputing.com/registermaps/.

4 Calibration

The PCI-DAS1000 is shipped fully-calibrated from the factory with calibration coefficients stored in nvRAM. At run time, these calibration factors are loaded into system memory and are automatically retrieved each time a different DAC/ADC range is specified. The user has the option to recalibrate with respect to the factory-measured voltage standards at any time by selecting the "Calibrate" option in InstaCal. Full calibration typically requires less than two minutes and requires no other user intervention.

4.1 Calibration Configuration - Analog Inputs

The PCI-DAS1000 provides self-calibration for the analog input and measurement circuits, eliminating the need for external equipment and user adjustments. All adjustments are made via 8-bit calibration DACs or 7-bit digital potentiometers referenced to an on-board factory-calibrated standard. Calibration factors are stored on the serial nvRAM.

A variety of methods are used to calibrate the different elements on the board. The analog front-end has several software “knobs” to turn. Offset calibration is performed in the instrumentation amplifier gain stage. Front-end gain adjustment is performed via a variable attenuator/gain stage.

Figure 4-1 is a block diagram of the analog input front-end calibration system:

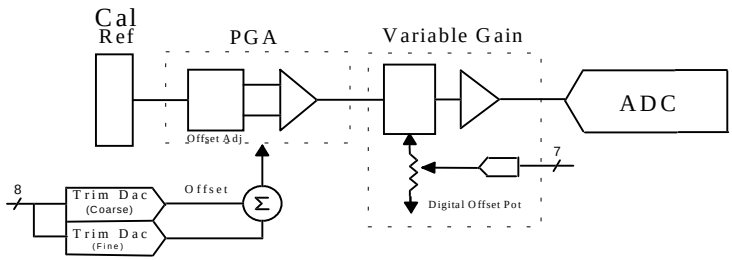


Figure4-1. Analog Front-End Calibration Block Diagram

4.2 Calibration Configuration - Analog Outputs (PCI-DAS1001 & PCI-DAS1002 Only)

The calibration scheme for analog outputs is in Figure 4-2. The function is duplicated for DAC0 and DAC1.

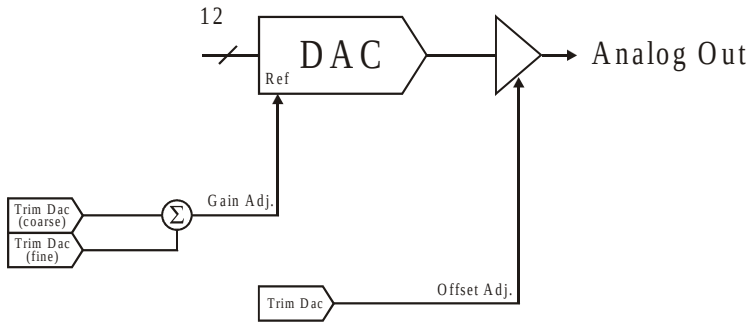


Figure 4-2. Analog Output Calibration Block Diagram - PCI-DAS1001 and PCI-DAS1002 Only

5 Specifications: PCI-DAS1000 & 1001

Typical for 25°C unless otherwise specified

Power Consumption

+5V Operating (A/D converting to FIFO)	0.8A typical, 1.0A max

Analog input Section

A/D converter type	7800
Resolution	12 bits
Number of channels	8 differential or 16 single-ended, software selectable
Input Ranges PCI-DAS1000 PCI-DAS1001	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V fully programmable ±10V, ±1V, ±0.1V, ±0.01V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V fully programmable
Polarity	Unipolar/Bipolar, software selectable
A/D pacing	Programmable: internal counter or external source (A/D External Pacer, positive or negative edge selectable by software) or software polled
Burstmode PCI-DAS1000 PCI-DAS1001	 Software selectable option, rate = 4µs Software selectable option, rate = 6.67µs
A/D Trigger sources	External digital (A/D External Trigger)
A/D Triggering Modes Digital: Pre-trigger: Data transfer: A/D conversion time:	 Software enabled, rising edge**,** hardware trigger Unlimited pre- and post-trigger samples. Total # of samples must be > 512. From 1024-sample FIFO via REPINSW, interrupt, or software polled 3 µs

Throughput	
PCI-DAS1001	150 kHz
PCI-DAS1000	250 kHz
Relative Accuracy	±1.5 LSB
Differential Linearity error:	±0.75 LSB
Integral Linearity error	±0.5 LSB typ, ±1.5 LSB max
Gain Error (relative to calibration reference)	
0.01V Range	± 0.4% of reading Max
All other Ranges	± 0.02% of reading Max
No missing codes guaranteed	12 bits
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM
Gain drift (A/D specs)	±6ppm/°C
Zero drift (A/D specs)	±1ppm/°C
Common Mode Range	±10V
CMRR @ 60Hz	70dB
Input leakage current	200nA
Input impedance	10Meg Ohms Min
Absolute maximum input voltage	
PCI-DAS1001	±35V
PCI-DAS1000	Channels 1-15: -40V to +55V power on or off Channel 0 : ±15V
Noise Distribution (Rate = 1-250KHz, Average % ±2 bins, Average % ±1 bin, Average # bins)	
PCI-DAS1000	
All Bipolar ranges	100% / 99.5% / 4 bins
All Unipolar ranges	100% / 99% / 5 bins
PCI-DAS1001	
10V Ranges	3 bins (100%)
1V Ranges	4 bins (100%)
0.1V Ranges	10 bins (100%)
Bipolar 0.01V Range	20 bins (100%)
Unipolar 0.01V Range	32 bins (100%)

Analog Output (PCI-DAS1001 only)

D/A type	AD7847AR
Resolution	12 bits
Number of channels:	2
Output Ranges	±10V, ±5V, 0 to 5V, 0 to 10V. Each channel independently programmable.

D/A pacing	Software
Data transfer	Programmed I/O.
Offset error	±600µV max, all ranges (calibrated)
Gain error	±0.02% FSR max (calibrated)
Differential nonlinearity	±1LSB max
Integral nonlinearity	±1LSB max
Monotonicity	12 bits
D/A Gain drift	±2 ppm/°C max
D/A Bipolar offset drift	±5 ppm/°C max
D/A Unipolar offset drift	±5 ppm/°C max

Throughput	PC-dependent
Settling time (to 0.01% of 10V step):	4µs typ
Slew Rate	7V/µS

Current Drive	±5 mA min
Output short-circuit duration	25 mA indefinite
Output Coupling	DC
Amp Output Impedance	0.1 Ohms max

Miscellaneous	Power up and reset, all DAC's cleared to 0 volts, ±200mV

Digital Input / Output

Digital Type	82C55A
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ –2.5mA
Output Low	0.4 volts max @ 2.5 mA
Input High	2.0 volts min, +5.5 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)
Interrupts	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable
Interrupt sources	Residual counter, End-of-channel-scan, AD-FIFO-not-empty, AD-FIFO-half-full

Counter section

Counter type	82C54
Configuration	Two 82C54 devices. 3 down counters per 82C54, 16 bits each
82C54A:	Counter 0: ADC residual sample counter. Source: ADC Clock Gate: Internal programmable source Output: End-of-Acquisition interrupt Counter 1: ADC Pacer Lower Divider Source: 10 MHz oscillator Gate: Tied to Counter 2 gate, programmable source. Output: Chained to Counter 2 Clock. Counter 2: ADC Pacer Upper Divider Source: Counter 1 Output. Gate: Tied to Counter 1 gate, programmable source. Output: ADC Pacer clock (if software selected), available at user connector (A/D Internal Pacer Output).

82C54B:	Counter 0: Pretrigger Mode Source: ADC Clock. Gate: External trigger Output: End-of-Acquisition interrupt Counter 0 - User Counter 4 (when in non-Pretrigger Mode) Source: User input at 100pin connector (CTR4 CLK) or internal 10MHz (software selectable) Gate: User input at 100pin connector (CTR4 GATE) Output: Available at 100pin connector (CTR4 OUT) Counter 1: User Counter 5 Source: User input at 100pin connector (CTR5 CLK) Gate: User input at 100pin connector (CTR5 GATE) Output: Available at 100pin connector (CTR5 OUT) Counter 2: User Counter 6 Source: User input at 100pin connector (CTR6 CLK) Gate: User input at 100pin connector (CTR6 GATE) Output: Available at 100pin connector (CTR6 OUT)
Clock input frequency	10 Mhz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	–40 to 100°C
Humidity	0 to 90% non-condensing

6 Specifications: PCI-DAS1002

Typical for 25°C unless otherwise specified.

Power consumption

+5V	0.8A typical, 1.0A max

Analog input section

A/D converter type	ADS7800 or equivalent
Resolution	12 bits
Number of channels	16 single-ended / 8 differential, software selectable
Input ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V software programmable
A/D pacing (software programmable)	Internal counter - 82C54.
	External source (A/D External Pacer) software programmable for rising or falling edge
	Software polled
A/D trigger sources	External edge trigger (A/D External Trigger)
A/D triggering modes	Rising or falling edge trigger - software selectable
A/D pre-trigger mode	Unlimited pre- and post-trigger samples. Total number of samples must be greater than 512.
Burst mode	Software selectable option, burst rate = 150kHz
Data transfer	From 1024 sample FIFO via REPINSW
	Programmed I/O
A/D conversion time	3µs max
Analog front end settling time	6µs for a full scale step to 1 LSB
Calibrated throughput	200KHz
Calibration	Auto-calibration, calibration factors for each range stored on board in nonvolatile RAM

Accuracy

Accuracies are listed for a 200KHz sampling rate, 100 sample average, single channel operation, a 15 minute warm-up, and operational temperatures within ±2degC of internal calibration temperature. The calibrator test source high side is tied to Channel 0 In and the low side tied to AGND.

Table 1 **– *Absolute Accuracy***

Range	Absolute Accuracy
±10.00V	±2.5 LSB max
±5.000V	±2.5 LSB max
±2.500V	±2.5 LSB max
±1.250V	±2.5 LSB max
0 to 10.00V	±2.5 LSB max
0 to 5.000V	±2.5 LSB max
0 to 2.500V	±2.5 LSB max
0 to 1.250V	±2.5 LSB max

Each PCI-DAS1002 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in *Table 1* above.

Table 2 **– *Calibrated Accuracy Components (in LSB)***

Range	Gain Error	Offset Error	DLE	ILE
All ranges	±1.0 max	±1.0 max	±0.75 max	±0.5 max

As shown in *Table 2*, total board error is a combination of Gain, Offset, Differential Linearity and Integral Linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full scale 100Hz triangle wave is input on Channel 1; Channel 0 is tied to Analog Ground at the 100 pin user connector. The table below summarizes the influence of Channel 1 on Channel 0 with the effects of noise removed. The residue on Channel zero is described in LSB's.

Condition	Crosstalk	Per channel Rate	ADC Rate
All Ranges	2 LSB_{pk-pk}	100 KHz	200 KHz

A/D Full-Scale Gain drift	±0.25 LSB/°C max
A/D Zero drift	±0.25 LSB/°C max
Common Mode Range	±10V min
CMRR @ 60Hz	-70dB min
Input leakage current	±20nA max
Input impedance	10 MOhms min
Absolute maximum input voltage	±35 volts
Warm-up time	15 minutes

Noise Performance

Table 3 below summarizes the noise performance for the PCI-DAS1002. Noise distribution is determined by gathering 50K samples at 200kHz with inputs tied to ground at the user connector.

Table 3 – *Board Noise Performance*

Range	% within ±2 LSB	% within ±1 LSB	LSBs	LSBrms*
0 to 1.250V	100%	99%	4	0.61
All other ranges	100%	100%	3	0.45

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6

Analog output section

D/A converter type	AD7847AR or equivalent
Resolution	12 bits
Number of channels	2
Configuration	Voltage Output, Single-ended
Output Range	±10V, ±5V, 0 to 10V, or 0 to 5V. Software selectable. Each channel independently programmable.
D/A pacing	Software
Data transfer	Programmed I/O

Absolute Accuracy

All Ranges	±3 LSB

Calibrated Accuracy Components

Gain Error	±1.0 LSB max
Offset Error	±0.5LSB max
Integral Linearity Error	±1.0 LSB max
Differential Linearity Error	±1.0 LSB max

Each PCI-DAS1002 is tested at the factory to assure absolute accuracy.

Total board error is a combination of Gain, Offset, Integral Linearity and Differential Linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a ±3.5 LSB error, our testing assures this error is never realized in a board that we ship.

Monotonicity	Guaranteed monotonic over temperature
Overall Analog Output drift	±0.03 LSB/°C max
Settling time	4µs to 0.01% of 10V step
Slew Rate	7V/µs min
Current Drive	±5 mA min
Output short-circuit duration	Indefinite @25mA
Output coupling	DC
Output impedance	0.1 ohms max
Miscellaneous	Double buffered output latches
	Output voltage on power up and reset: ±200mV

Counter section

Counter type	82C54	
Configuration	Two 82C54 devices, 3 down counters per 82C54, 16 bits each	
Counter 1 – ADC residual sample counter	Source:	ADC clock
	Gate:	Internal programmable source
	Output:	End of acquisition interrupt
Counter 2 - ADC Pacer Lower Divider	Source:	10 MHz internal source
	Gate:	Internal, programmable on/off
	Output:	Chained to Counter 3 Clock
Counter 3 - ADC Pacer Upper Divider	Source:	Counter 2 Output
	Gate:	Internal, programmable on/off
	Output:	Programmable as ADC Pacer clock. Available at user connector (ADC Pacer out)
Counter 4 – Pre-trigger mode	Source:	ADC clock for pre-trigger mode
	Gate:	External trigger for pre-trigger mode
	Output:	End of acquisition interrupt for pre-trigger mode
Counter 4 – Non-Pre-Trigger mode	Source:	External at connector (CTR4 CLK)
	Gate:	External at connector (CTR4 GATE)
	Output:	Available at connector (CTR4 OUT)
Counter 5 - User counter	Source:	External at connector (CTR5 CLK)
	Gate:	External at connector (CTR5 GATE)
	Output:	Available at connector (CTR5 OUT)
Counter 6 - User counter	Source:	External at connector (CTR6 CLK)
	Gate:	External at connector (CTR6 GATE)
	Output:	Available at connector (CTR6 OUT)
Clock input frequency	10Mhz max	
High pulse width (clock input)	30ns min	
Low pulse width (clock input)	50ns min	
Gate width high	50ns min	
Gate width low	50ns min	
Input low voltage	0.8V max	
Input high voltage	2.0V min	
Output low voltage	0.4V max	

Output high voltage	3.0V min
Crystal Oscillator Frequency	10MHz
Frequency accuracy	50ppm

Digital input/output section

Digital Type	82C55
Number of I/O	24 (Port A0 through Port C7)
Configuration	• 2 banks of 8 and 2 banks of 4 or
	• 3 banks of 8 or
	• 2 banks of 8 with handshake
Input high voltage	2.0V min, 5.5V absolute max
Input low voltage	0.8V max, –0.5V absolute min
Output high voltage (IOH = -2.5mA)	3.0V min
Output low voltage (IOL = 2.5mA)	0.4V max
Power-up / reset state	Input mode (high impedance)

Interrupt section

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable. Default = disabled.
Interrupt sources	• Residual sample counter • A/D End-of-channel-scan • A/D FIFO-not-empty • A/D FIFO-half-full • A/D Pacer

Miscellaneous

+5 Volts	Available at I\O connector (PC+5V)
+12 Volts	Available at I\O connector (PC +12V)
-12 Volts	Available at I\O connector (PC –12V)

Environmental

Operating Temperature Range	0 to 70°C
Storage Temperature Range	-40 to 100°C
Humidity	0 to 95% non-condensing

Mechanical

Card dimensions	PCI half card: 174.63mm(L) x 106.86mm(H) x 14.48mm(D)

Connector and Pin Out

8 Channel Differential Mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRST PORT A 0
2	CH0 HI	52	FIRST PORT A 1
3	CH0 LO	53	FIRST PORT A 2
4	CH1 HI	54	FIRST PORT A 3
5	CH1 LO	55	FIRST PORT A 4
6	CH2 HI	56	FIRST PORT A 5
7	CH2 LO	57	FIRST PORT A 6
8	CH3 HI	58	FIRST PORT A 7
9	CH3 LO	59	FIRST PORT B 0
10	CH4 HI	60	FIRST PORT B 1
11	CH4 LO	61	FIRST PORT B 2
12	CH5 HI	62	FIRST PORT B 3
13	CH5 LO	63	FIRST PORT B 4
14	CH6 HI	64	FIRST PORT B 5
15	CH6 LO	65	FIRST PORT B 6
16	CH7 HI	66	FIRST PORT B 7
17	CH7 LO	67	FIRST PORT C 0
18	LLGND	68	FIRST PORT C 1
19	N/C	69	FIRST PORT C 2
20	N/C	70	FIRST PORT C 3
21	N/C	71	FIRST PORT C 4
22	N/C	72	FIRST PORT C 5
23	N/C	73	FIRST PORT C 6
24	N/C	74	FIRST PORT C 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	CTR5 CLK
36	D/A OUT 0	86	CTR5 GATE
37	D/A GND 1	87	CTR5 OUT
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

16 Channel Single-Ended Mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRST PORT A 0
2	CH0 HI	52	FIRST PORT A 1
3	CH8 HI	53	FIRST PORT A 2
4	CH1 HI	54	FIRST PORT A 3
5	CH9 HI	55	FIRST PORT A 4
6	CH2 HI	56	FIRST PORT A 5
7	CH10 HI	57	FIRST PORT A 6
8	CH3 HI	58	FIRST PORT A 7
9	CH11 HI	59	FIRST PORT B 0
10	CH4 HI	60	FIRST PORT B 1
11	CH12 HI	61	FIRST PORT B 2
12	CH5 HI	62	FIRST PORT B 3
13	CH13 HI	63	FIRST PORT B 4
14	CH6 HI	64	FIRST PORT B 5
15	CH14 HI	65	FIRST PORT B 6
16	CH7 HI	66	FIRST PORT B 7
17	CH15 HI	67	FIRST PORT C 0
18	LLGND	68	FIRST PORT C 1
19	N/C	69	FIRST PORT C 2
20	N/C	70	FIRST PORT C 3
21	N/C	71	FIRST PORT C 4
22	N/C	72	FIRST PORT C 5
23	N/C	73	FIRST PORT C 6
24	N/C	74	FIRST PORT C 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	CTR5 CLK
36	D/A OUT 0	86	CTR5 GATE
37	D/A GND 1	87	CTR5 OUT
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the products:

Part Number	Description
PCI-DAS1000	High speed analog input board for the PCI bus
PCI-DAS1001	High speed analog input board for the PCI bus
PCI-DAS1002	High speed analog input board for the PCI bus

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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