Specifications

PCI-DAS1002

Revision 1.2, June, 2005

Specifications

Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input section

Table 1. Analog input specifications

Parameter	Specification
A/D converter type	ADS7800 or equivalent
Resolution	12 bits
Number of channels	16 single-ended / 8 differential, software selectable
Input ranges	±10 V, ±5 V, ±2.5 V, ±1.25 V, 0 to 10 V, 0 to 5V, 0 to 2.5 V, 0 to 1.25 V software programmable
A/D pacing (software programmable)	Internal counter - 82C54.
	External source (A/D External Pacer) software programmable for rising or falling edge
	Software polled
A/D trigger sources	External edge trigger (A/D EXTERNAL TRIGGER)
A/D triggering modes	Rising edge trigger
A/D pre-trigger mode	Unlimited pre- and post-trigger samples. Total number of samples must be greater than 512.
Burst mode	Software selectable option, burst rate = 150 kHz
Data transfer	From 1024 sample FIFO via REPINSW
	Programmed I/O
A/D conversion time	*3 µs max*
Analog front end settling time	*6 µs for a full scale step to 1 LSB*
Calibrated throughput	200 kHz
Calibration	Auto-calibration, calibration factors for each range stored on board in nonvolatile RAM
A/D full-scale gain drift	±0.25 LSB/°C max
A/D zero drift	±0.25 LSB/°C max
Common mode range	±10 V min
CMRR @ 60 Hz	-70 dB min
Input leakage current	*±20 nA max*
Input impedance	*10 MOhms min*
Absolute maximum input voltage	*±35 volts*
Warm-up time	*15 minutes*

Accuracy

Accuracies are listed for a 200 kHz sampling rate, 100 sample average, single channel operation, a 15 minute warm-up, and operational temperatures within ±2 °C of internal calibration temperature. The calibrator test source high side is tied to Channel 0 In and the low side tied to AGND.

Table 2. Absolute accuracy specifications (analog input)

Range	Absolute Accuracy
±10.00 V	±2.5 LSB max
±5.000 V	±2.5 LSB max
±2.500 V	±2.5 LSB max
±1.250 V	±2.5 LSB max
0 to 10.00 V	±2.5 LSB max
0 to 5.000 V	±2.5 LSB max
0 to 2.500 V	±2.5 LSB max
0 to 1.250 V	±2.5 LSB max

Each PCI-DAS1002 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2 above.

Table 3. Calibrated accuracy components (in LSB)

Range	Gain Error	Offset Error	DLE	ILE
All ranges	±1.0 max	±1.0 max	±0.75 max	±0.5 max

As shown in Table 3, total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full scale 100 Hz triangle wave is input on channel 1; Channel 0 is tied to analog ground at the 100-pin user connector. The table below summarizes the influence of channel 1 on channel 0 with the effects of noise removed. The residue on channel zero is described in LSB's.

Table 4. Crosstalk specifications

Condition	Crosstalk	Per channel Rate	ADC Rate
All ranges	2 LSB_{pk-pk}	100 kHz	200 kHz

Noise Performance

Table 5 below summarizes the noise performance for the PCI-DAS1002. Noise distribution is determined by gathering 50 K samples at 200 kHz with inputs tied to ground at the user connector.

Table 5. Board noise performance

Range	% within ±2 LSB	% within ±1 LSB	LSBs	LSBrms*
0 to 1.250 V	100%	99%	4	0.61
All other ranges	100%	100%	3	0.45

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

Analog output section

Table 6. Analog output specifications

D/A converter type	AD7847AR or equivalent
Resolution	12 bits
Number of channels	2
Configuration	Voltage output, single-ended
Output range	±10 V, ±5 V, 0 to 10 V, or 0 to 5 V. Software selectable. Each channel independently programmable.
D/A pacing	Software
Data transfer	Programmed I/O
Monotonicity	*Guaranteed monotonic over temperature*
Overall analog output drift	±0.03 LSB/°C max
Settling time	4 µs to 0.01% of 10 V step
Slew rate	7 V/µs min
Current drive	±5 mA min
Output short-circuit duration	*Indefinite @25 mA*
Output coupling	DC
Output impedance	0.1 Ohm, max
Miscellaneous	*Double buffered output latches*
	Output voltage on power up and reset: ±200 mV

Absolute accuracy

Table 7. Absolute accuracy specifications (analog output)

All ranges	±3 LSB

Calibrated accuracy components

Table 8. Calibrated accuracy specifications (analog output)

Gain error	±1.0 LSB max
Offset error	±0.5LSB max
Integral linearity error	±1.0 LSB max
Differential linearity error	*±1.0 LSB max*

Each PCI-DAS1002 is tested at the factory to assure absolute accuracy.

Total analog output error is a combination of gain, offset, integral linearity and differential linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a ±3.5 LSB error, our testing assures this error is never realized in a board that we ship.

Counter section

Table 9. Counter specifications

Counter type	82C54
Configuration	Two 82C54 devices, 3 down counters per 82C54, 16 bits each
Counter 1 — ADC residual sample counter	Source: ADC clock
	Gate: Internal programmable source
	Output: End of acquisition interrupt
Counter 2 — ADC pacer lower divider	Source: 10 MHz internal source
	Gate: Internal, programmable on/off
	Output: Chained to counter 3 clock
Counter 3 — ADC pacer upper divider	Source: Counter 2 output
	Gate: Internal, programmable on/off
	Output: Programmable as ADC pacer clock. Available at user connector (ADC pacer out)
Counter 4 — Pre-trigger mode	Source: ADC clock for pre-trigger mode
	Gate: External trigger for pre-trigger mode
	Output: End of acquisition interrupt for pre-trigger mode
Counter 4 — Non pre-trigger mode	Source: External at connector (CTR4 CLK)
	Gate: External at connector (CTR4 GATE)
	Output: Available at connector (CTR4 OUT)
Counter 5 — User counter	Source: External at connector (CTR5 CLK)
	Gate: External at connector (CTR5 GATE)
	Output: Available at connector (CTR5 OUT)
Counter 6 — User counter	Source: External at connector (CTR6 CLK)
	Gate: External at connector (CTR6 GATE)
	Output: Available at connector (CTR6 OUT)
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*30 ns min*
Low pulse width (clock input)	*50 ns min*
Gate width high	*50 ns min*
Gate width low	*50 ns min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*
Crystal oscillator frequency	10 MHz
Frequency accuracy	50 ppm

Digital input/output section

Table 10. DIO specifications

Digital type	82C55
Number of I/O	24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7)
Configuration	2 banks of 8 and 2 banks of 4 or
	3 banks of 8 or
	2 banks of 8 with handshake
Input high voltage	*2.0 V min, 5.5 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage (IOH = -2.5 mA)	*3.0 V min*
Output low voltage (IOL = 2. 5mA)	*0.4 V max*
Power-up / reset state	Input mode (high impedance)

Interrupt section

Table 11. Interrupt specifications

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable. Default = disabled.
Interrupt sources	Residual sample counter A/D End-of-channel-scan A/D FIFO-not-empty A/D FIFO-half-full A/D Pacer

Miscellaneous

Table 12. Micellaneous specifications

+5 Volts	Available at I\O connector (PC +5V)
+12 Volts	Available at I\O connector (PC +12V)
-12 Volts	Available at I\O connector (PC –12V)

Power consumption

Table 13. Power consumption specifications

+5 V	0.8 A typical, 1.0 A max

Environmental

Table 14. Environmental specifications

Operating temperature range	0 to 70°C
Storage temperature range	-40 to 100°C
Humidity	0 to 95% non-condensing

Mechanical

Table 15. Mechanical specifications

Card dimensions	PCI half card: 174.63 mm (L) x 106.86 mm (H) x 14.48 mm (D)

Connector and pin out

Table 16. Main connector specifications

Connector type	100-pin high-density Robinson Nugent	
Compatible cable	C100FF-x, unshielded ribbon cable, x =3 or 6 feet	
Compatible accessory products (with C100FF-x cable)	ISO-RACK16/P ISO-DA02/P CIO-ERB24 (DADP-5037 adaptor required) CIO-SERB24/FD (DADP-5037 adaptor required) SSR-RACK24 (DADP-5037 adaptor required)	BNC-16SE BNC-16DI CIO-MINI50 (2 required) CIO-TERM100 (1 required) SCB-50 (1 required)

Table 17. 8-channel differential mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH0 LO	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH1 LO	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH2 LO	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH3 LO	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH4 LO	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH5 LO	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH6 LO	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH7 LO	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	CTR5 CLK
36	D/A OUT 0	86	CTR5 GATE
37	D/A GND 1	87	CTR5 OUT
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

Table 18. 16-channel single-ended mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH8 HI	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH9 HI	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH10 HI	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH11 HI	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH12 HI	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH13 HI	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH14 HI	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH15 HI	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	CTR5 CLK
36	D/A OUT 0	86	CTR5 GATE
37	D/A GND 1	87	CTR5 OUT
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com